Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) Method of forming a transistor comprising:
disposing a planar platform of silicon atop a support structure of oxide which is atop a substrate;
wherein the support structure is disposed beneath the planar platform;
forming gate structures both atop and beneath the planar platform; and
forming source and drain diffusions within the planar platform; and
forming multiple gate structures atop the planar platform.

2. (Original) Method, according to claim 1, wherein:
the gate structures which are formed beneath the planar platform are smaller than the planar platform.

3. (Original) Method, according to claim 1, wherein:
the gate structures which are formed beneath the planar platform are aligned with the gate structures which are formed atop the planar platform.

Claims 4-10 (canceled)

11. (previously presented) Method of forming a transistor comprising:
providing an SOI wafer comprising a handle substrate, a buried oxide layer (BOX) disposed atop the handle substrate and a silicon-on-insulator (SOI) layer disposed atop the buried oxide layer;
in a first etching step, patterning the SOI layer to become the active silicon layer of an SOI transistor, wherein a portion of the buried oxide layer is underneath the patterned SOI layer and other portions of the buried oxide layer are not underneath the patterned SOI layer, and wherein a top surface of the patterned SOI layer is exposed;
in a second etching step, etching the portions of the buried oxide layer which are not underneath the patterned SOI layer, thereby exposing a portion of a top surface of the handle substrate;
in a third etching step, removing the buried oxide layer from under the patterned SOI layer to form a standoff structure, thereby exposing a portion of a bottom surface of the patterned SOI layer;
performing gate oxidation, thereby forming gate oxide on the exposed surfaces of the patterned SOI layer;
depositing gate electrode material atop the handle substrate and covering the standoff structure as well as the patterned SOI layer; and
in a fourth etching step, etching the gate electrode material to form at least one gate stack atop the patterned SOI layer.

12. (previously presented) Method, according to claim 11, further comprising:
in a fifth etching step, etching the gate electrode material to form a back gate beneath the patterned SOI layer.

13. (Original) Method, according to claim 11, wherein:
the back gate is aligned with the at least one gate stack.

14. (previously presented) Method, according to claim 11, wherein:
the third etching step exposes a substantial portion of the underside of the patterned SOI layer.

15. (previously presented) Method, according to claim 11, wherein:
the third etching step exposes approximately 80% of the underside of the patterned SOI layer.

16. (Original) Method, according to claim 11, wherein:
the third etching step exposes additional portions of the handle substrate.

17. (Original) Method, according to claim 11, wherein:
during gate oxidation, gate oxide is also formed on the exposed surface of the handle substrate.

18. (Original) Method, according to claim 11, further comprising:
prior to the fourth etching step, depositing a hard mask material on top of the gate electrode material;
defining the hard mask material;
then performing the fourth etching step;
then removing the hard mask.

19. (original) Method, according to claim 11, wherein:
the gate stack is etched in the fourth etching step using an anisotropic dry etch that is selective to the gate oxide.

20. (previously presented) Method, according to claim 11, wherein:
in the fourth etching step, the gate electrode material is etched down to approximately the level of the top surface of the patterned SOI layer, thereby creating electrode structures atop the patterned SOI layer and isolated therefrom by gate oxide.

21. (original) Method, according to claim 1, wherein:
the platform of silicon is supported from below by the support structure.

22. (currently amended) Method, according to claim 1, wherein:
the support structure is centered under the planar platform of silicon.

23. (currently amended) Method, according to claim 1, wherein:
the ~~standoff~~ support structure ~~is a portion of the oxide which is atop the substrate~~ is 10-100 nm wide and approximately 200nm high.

24. (canceled)

25. (currently amended) Method, according to claim 1, wherein:
~~before forming the gate structures,~~ the support structure is in contact with the underside of the planar platform, leaving approximately 80% of an underside of the planar platform is exposed.

26. (original) Method, according to claim 1, wherein:
the gate structures which are formed beneath the planar platform are smaller than the planar platform.

27. (original) Method, according to claim 1, wherein:
the gate structures which are formed beneath the planar platform are aligned with the gate structures which are formed atop the planar platform.